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In the USPTO

In Re Application of loan DANCEA

Filed: May 15, 2001

Priority: CA 2,338,458

For:" METHOD AND VLSI CIRCUITS ALLOWING TO CHANGE DYNAMICALLY THE LOGICAL BEHAVIOUR"

INFORMATION DISCLOSURE STATEMENT

The Commissioner for Patents
Washington, D.C. 20231

Sir:

I submit herewith patents, publications, and other Information of which I am aware or believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

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Statement of Relevancy

RE: "Dynamically Changing the Logical Behavior of a Microcomputer Interface" IEEE MICRO, April 1989

1. This article published in 1989 has marked the beginning of a long search for a real invention. The article does not include any real hardware solution because the invention was not ready at the time. They are errors in the article, as for example:

a. The statement at p.50, first paragraph right and Figure 12 that the idea disclosed in the article may be used, as the basis for developing a VLSI circuit is false. The correct solution is exemplified in the patent disclosure, particularly in Figures 3, 4, 6 and 7.

b. The article does not mentioned what type of VLSI circuit can take advantage of the invention. The present patent application provides the hardware structure of three new types of VLSI circuits, having re-configurable logic behavior. A first embodiment implements any type of multiple output combinational circuit, a second embodiment implements any synchronous sequential circuit with only clock input and, a third embodiment implements any synchronous sequential circuits with data input and clock input.

c. The "basic cell" in Figure 12 of the mentioned article has several mistakes. Firstly, the OR "ports" (really OR gates) are not part of the basic cell (see the description in the patent disclosure). With the OR gates placed in the basic cell, the logical behavior of the structure is completely erroneous.

Secondly, the "comparator" block is not appropriate in the structure of the basic cell. When dealing with a large number of input bits, the structure of the comparator needs a huge increasing of the hardware (several times the number of gates used for the remainder of basic cell). For this reason, in the patent disclosure the comparator was replaced by a set of XNOR gates followed by a single AND gate.

Thirdly, the "Control block" mentioned in the Figure 12 of the article is erroneous; for example no necessary any connection of type CS (chip select).

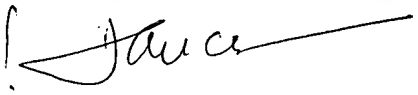
Fourthly, the word "ports", which refer to input/output communication and consequently to a specific hardware structure, was used throughout the block labeling of Figure 12, instead of the word gates, fact that is incorrect and can produce confusions.

2. In addition, in 1989 the available technology for manufacturing VLSI circuits was less advanced and there was no practical solution to my inventive idea as the implementation of such structure would have require a very large real estate and an increased price.

3. I was discouraged because I knew there is something deficient in the initial general concept, and because the implementation step appeared to be so remote. I diligently pursued my idea as I am convinced it is a progress in digital hardware technology, is new and useful, as well as feasible at affordable prices under present technology advancements.

4. I retired last year from "University of Quebec at Hall" and I revisited the concept. Now I know how the invention works and the last test needed to show operability has been completed. Consequently, I applied for a patent.

Respectfully submitted,
Prof. loan Dancea
May 29, 2001, Ottawa, CANADA



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Application Number	
Filing Date	
First Named Inventor	
Group Art Unit	
Examiner Name	
Attorney Docket Number	

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,361,373		GILSON et al	11-01-1994	
		5,995,744		GUCCIONE et al	11-30-1999	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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Attorney Docket Number	

09/874027 jc678 U.S.PTO 06/06/01

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		IOAN DANCEA "Dynamically Changing the Logical Behavior of a Microcomputer Interface", IEEE MICRO, April 1989, pg 39-51	

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